Mixed Signal Technologies Enabling PSOC and PSIP

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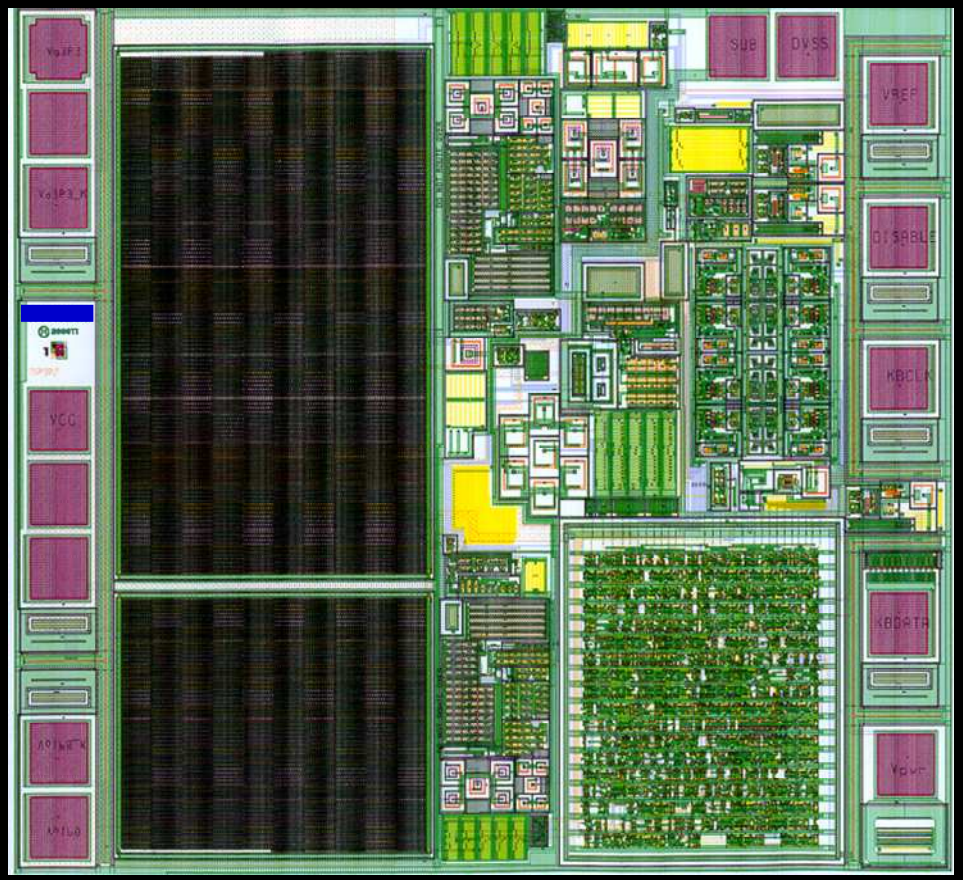
Typical Power Management IC

- Digital content
  - Controllers, Logic
- Analog content
  - Feedback, ADC, DAC, Fault detection/prevention, Sensing
- High voltage
  - Gate driver, charge pump, regulators
- Power
  - Linear regs, SMPS (boost, buck, flyback)
- Passives
  - Capacitors, Resistors



(Power)SOC & SIP

- Benefits
  - Utilization of the best controlled manufacturing process
  - Smallest size solution for complete application
  - Reduced manufacturing cost
  - Increased functionality, fault management and sensing

- Challenges
  - Process technology compatibility → integration of digital+analog+high voltage+power+passives
  - In-package thermal management
  - Circuit isolation and noise management
  - Metal interconnect and oxide voltage and reliability

Mixed Signal Technology Integration

- Digitization of Analog Functions
  - enabled by cheap gates
  - reduces power consumption
  - drives to defect limited yield
  - complex closed loop algorithm implementation

- Analog Characterization of "Digital Processes"
  - key to enable "system-on-a-chip" (even SIP)
  - analog "process control" for roadmap digital technology
  - digital transistor "adjustments" to meet analog circuit demands

Mixed Signal Technology Integration

- Total Mixed Signal Integration
  - integrate whatever that cannot be integrated on a DSP/MCU chip
  - cost focused – maximize analog and HV integration
  - process complexity to support specialized components
  - low/no incremental process cost and complexity exclusively for digital density
  - balanced process/component design & circuit design problem

Mixed Signal Technology Drivers

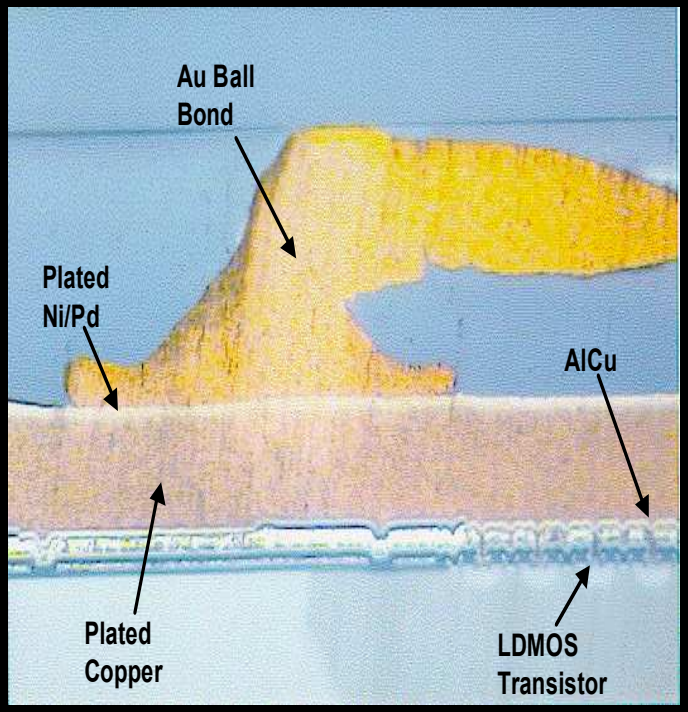
- Analog CMOS
  - low noise and improved matching (Leff <0.15um)
  - low Vt and low leakage
  - well characterized base analog CMOS building blocks
- Integrated HV and power devices
  - single/dual gate technology (Vt management)
  - variable voltage capability
  - variable voltage – high current carrying power device design

Mixed Signal Technology Drivers

- Integrated passives
  - well matched capacitors and resistors (magnetics?)
  - no area constraints, design flexibility
- Dielectric/junction isolation
  - separate analog and digital blocks for noise control
  - band gap, reference and sensing management
- Other components
  - higher voltage “analog friendly” cmos
  - HV and high performance bipolar devices, efficient diodes

Mixed Signal Technology Drivers

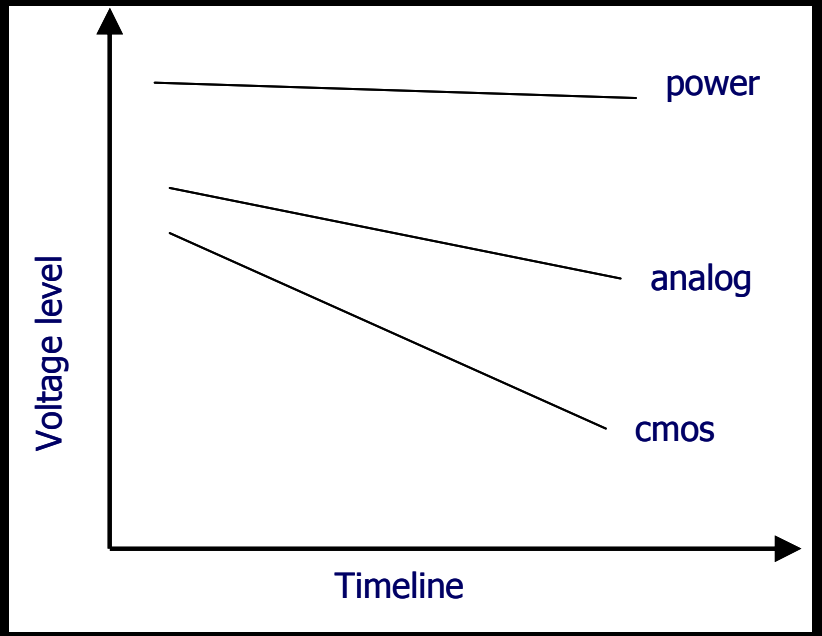
- High current capable power bussing/interconnect
  - bussing interconnect technology to reduce power device area (thick metal driver)
  - bond over active area



TI thick copper and bonding technology

Voltage Roadmap vs. Technology Platform

- CMOS & Logic roadmap
  - aggressive size reduction
  - aggressive voltage reduction (Efield scaling)
- Analog roadmap
  - slow size reduction
  - moderate voltage reduction
  - precision improvement and better passives
- Power roadmap
  - slow size reduction
  - voltage stability or increase
  - optimized power performance



Challenge: To develop a single **cost-effective** integrated technology

Process Direction

- **CMOS & Logic**
  - thin & low-k dielectrics
  - thinner & narrower metallization
  - multiple CMP metal levels
  - expensive deep submicron lithography
  - speed & power & density
  - shallow trench isolation (STI)
  - zero/minimal thermal budget
  - complex chain implants and sub-micron profiles
  - Ion/Ioff ratio driven
  - highly integrated
- **Analog & Power**
  - epitaxy (Si, SiGe)
  - thick copper metallization for current
  - CMP metal
  - SOI, buried layers, deep trench isolation, STI
  - standard lithography
  - power density & functionality
  - precision passives
  - deeper junctions
  - single/dual gate oxide
  - non-volatile solutions
  - modular integration

CMOS Roadmap and Power ICs

- **Pros**
  - salicide technology
  - trench etch & fill
  - CMP and W-plugs
  - MeV (high energy) implants
  - “resurf-like” wells
  - thick oxide field plates
  - improved alignment tolerance
  - better matching & parametric control
- **Cons**
  - thinner & low-k dielectrics
  - thinner metal system
  - very high doped wells
  - significantly reduced thermal cycle
  - thinner gate oxides
  - higher energy implants
  - increased process cost

Key Component Requirements

- Analog CMOS
  - compatible with high performance logic, modular features and low cost
  - "very good" analog DC characteristics
    - Vt. Gds. Gm. Delta-Vt, Ioff, Vdd
  - additional features
    - high voltage
    - low Vt, low leakage
  - excellent matching and 1/f noise and low dynamic Vt shift
  - isolate substrate and switching interference noises

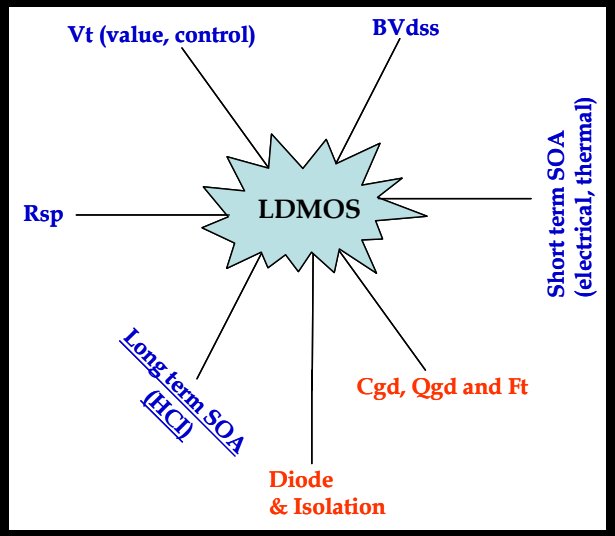
Key Component Requirements

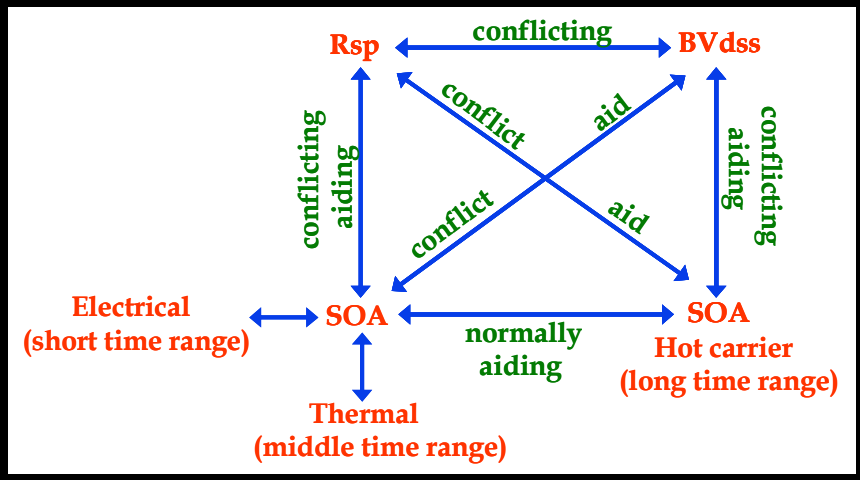
- High voltage & power
  - voltage scalability & isolation
  - modular and minimal process cost
  - current scalability
  - compatibility with high performance logic

➔**Drives**

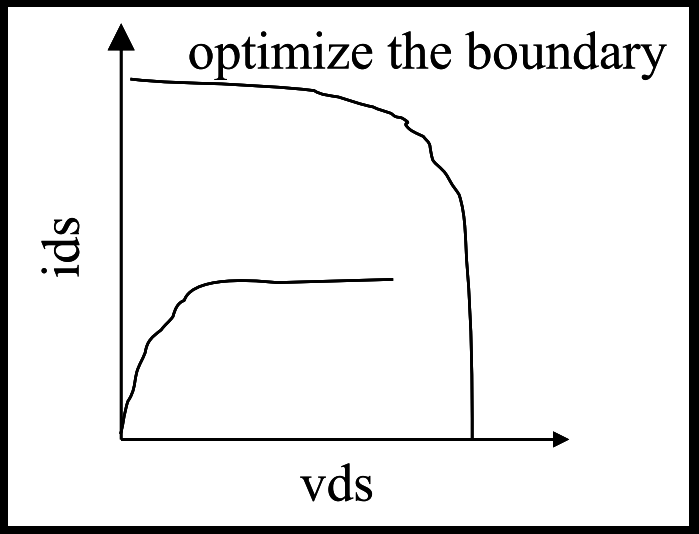
- MOS based solution
  - ease of integration & high i/p impedance
  - mostly uniform current flow & faster switching
- Lateral solution
  - easier to integrate
  - easier voltage scalability
  - normally lower Rdson X Qgate compared to vertical (lower Rdson)

Optimizing Power Devices

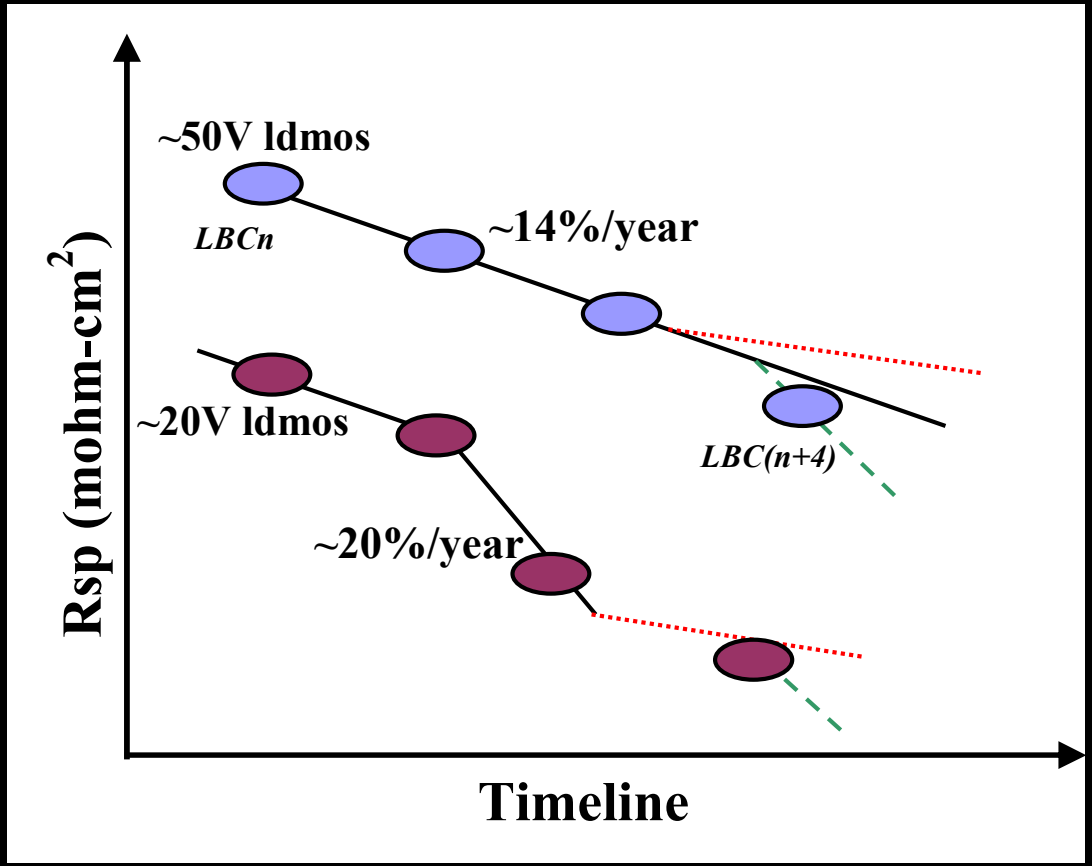




- Key HV device parameters
  - breakdown voltage (∞)
  - on-state resistance (0)
  - device robustness (intrinsic ∞)
  - switching speed (intrinsic ∞)
  - reliability (>> 10 years)

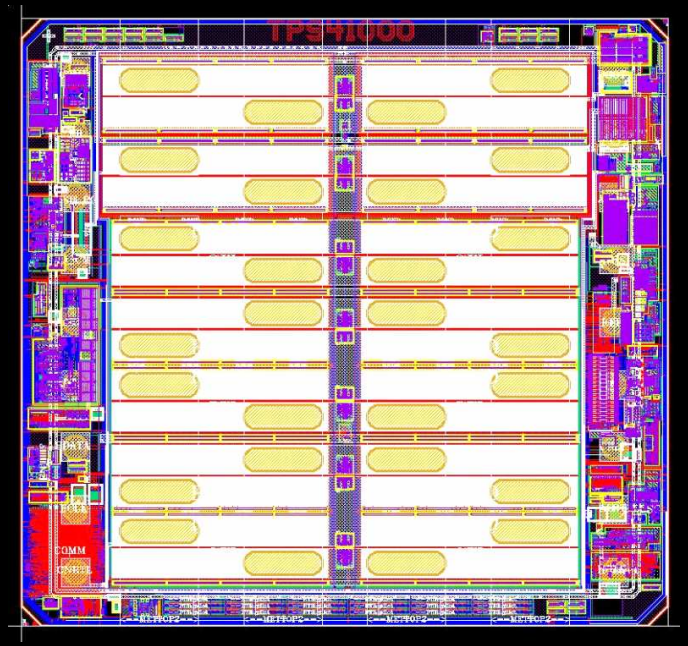


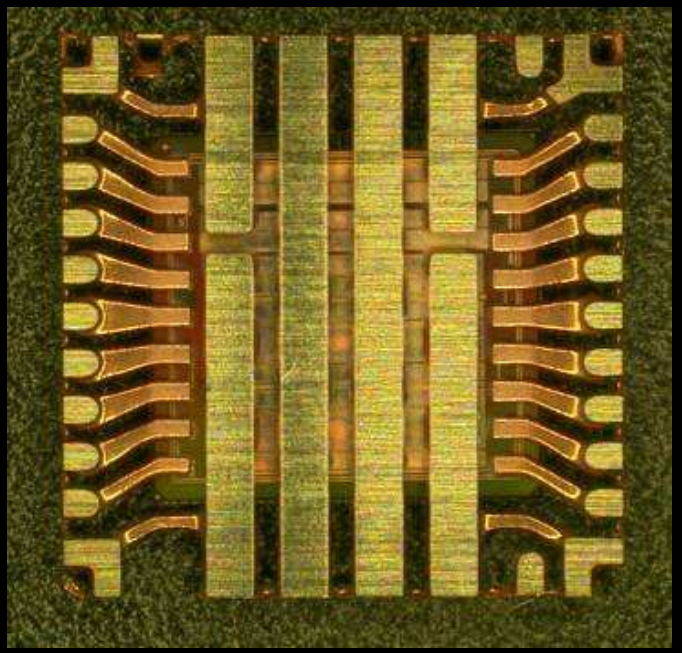
Integrated FET Scaling – Drives Technology



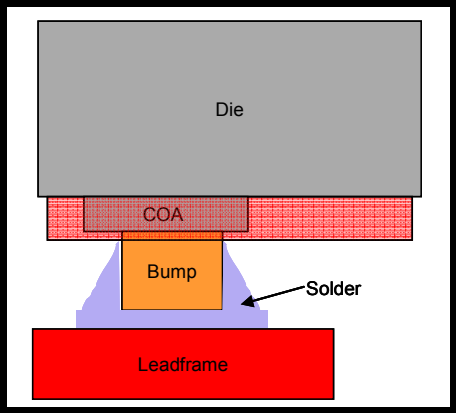
- Integrated FET improvement at TI
  - about 25-30% node-on-node improvement

Packaging Innovation –SOC/SIP power density

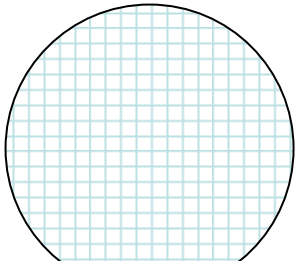




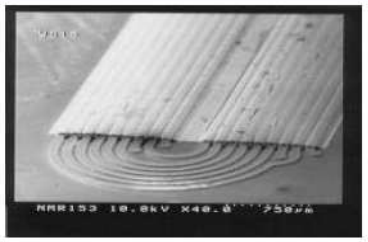
- Up to 20A monolithic dc-dc converter
  - enhanced thermal performance
  - no wires, low parasitics and high reliability



Passive integration

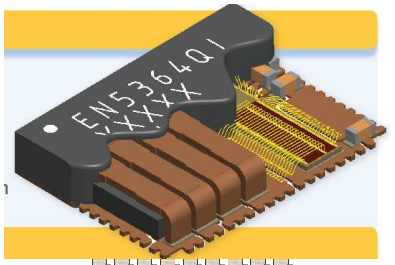


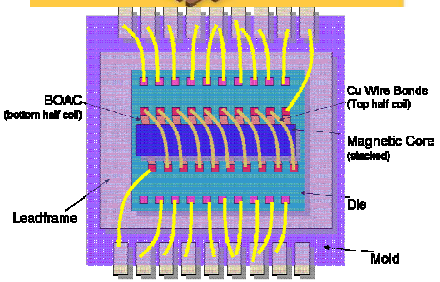
FAB Process



METTOP Process

Package Assembly IPDs





- Drives improved isolated and non-isolated power supplies (transformers and inductors)
- Drives high density capacitors – decoupling, precision
  - **<u>Enables full power supply in package</u>**

Summary

Logic + Analog + Power Innovation

+

Passive Integration

+

Packaging Innovation

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Manufacturing Base

Drive SOC and SIP